An Inverted Microstrip Line IC Structure for ultra high-speed Applications

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Abstract

An inverted microstrip line IC structure for ultra high-speed applications is proposed. It allows a very low-parasitic-impedance module with a flip-chip bonding, a small IC size, and performance improvements for high-speed digital ICs.

Introduction

ultra high-speed optical transmission systems are expected to be the backbone of future multimedia communications. 10-Gbit/s ICs and their modules were developed a few years ago, but even higher bit rates of around 40-Gbit/s are needed. There are, however, several serious problems in developing 40-Gbit/s IC modules with conventional metal QFP packages and bonding wire. Flip-chip bonding technology is necessary for reducing the parasitic impedance of ground and signal lines, and implementing the "chip size cavity package" concept [1] is indispensable in suppressing the cavity resonance of packages. Impedance-controlled and low-coupling transmission lines are required not only in analog circuits such as distributed amplifiers but also in high-speed digital ICs, because the length of signal lines is more than 1/10 of the signal wavelength at such high frequencies. Coplanar waveguide (CPW) lines have been used in high-density MMICs, but as described below, these are not suitable for high-speed digital ICs. This paper proposes a novel IMSL (Inverted Microstrip Line) / TPSL (Triplate Strip Line) –IC structure that is suitable for the flip-chip bonding module format.

IMSL-IC Structure

Figure 1 shows a schematic of the IMSL-IC structure. The IMSL–IC is constructed with two 10-μm-thick polyimide multilayers [2], and circuit elements such as FETs and resistors are fabricated on the GaAs substrate surface. There are a total of four metal layers. MIM capacitors are constructed from the two lower layers. For signal propagation, an IMSL and TPSL are used in addition to the conventional signal lines in first and second layers. The IMSL uses a third-layer strip with a top-layer ground plane. For the TPSL, a second-layer ground plane is added to the IMSL in order to enhance the signal-shielding effect.

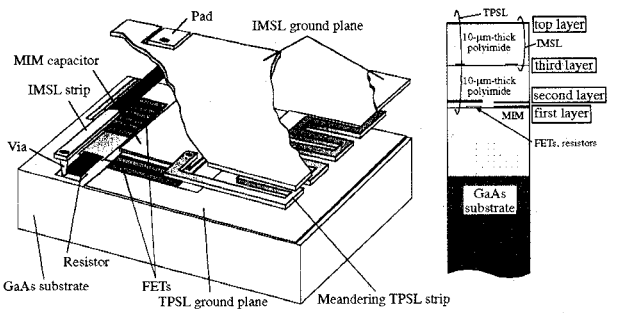

Figure 1: IMSL-IC structure.

Features of IMSL-IC

The most significant feature of this structure is that the entire top metal plane acts as a ground. The effect of this is apparent in the flip-chip bonding module format shown in Figure 2. IC ground impedance is kept extremely low by using many ground connecting bumps on the plane. This insures stable, low-jitter operation in high-speed modules. Moreover, the signal line parasitic effect is lower than in wire and ribbon connections.

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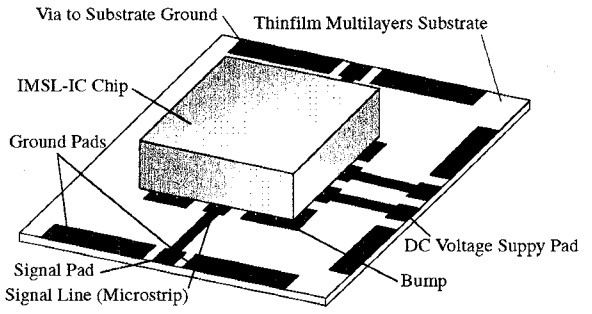


Figure 2: Flip-chip bonding module with IMSL-IC.

One of the problems with flip-chip bonding is that signal-line impedance changes when the chip is close to the substrate. This degrades module performance, especially impedance-sensitive gain blocks. The impedance changes calculated for an IMSL and for conventional CPW lines are shown in Figure 3. The changes for CPW lines are very large when the chip-substrate distance is less than 100 μm, and the selectivity of bump size will be quite restricted in this case. The top ground plane of the IMSL, however, eliminates this impedance change.

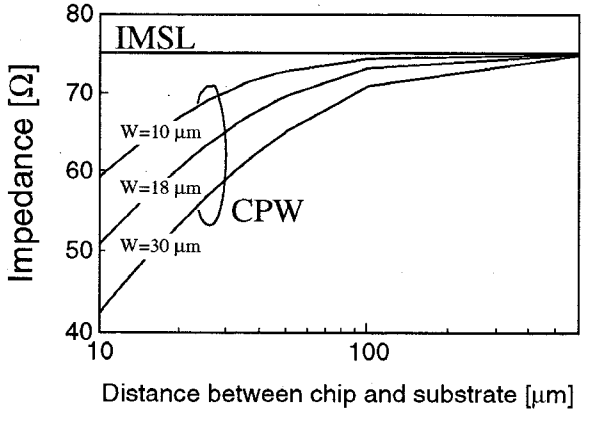


Figure 3: Impedance reduction with flip-chip bonding.

Another feature of the IMSL-IC structure is its excellent isolation characteristics. Simulated isolation characteristics of 500-μm -long IMSLs with a 5- to 20-μm space and experimental results with a 5-μm space are shown in Figure 4.

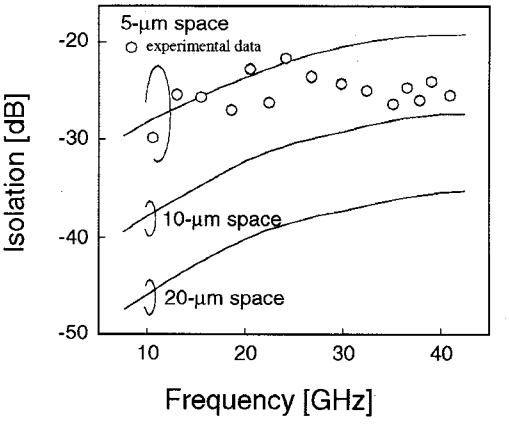


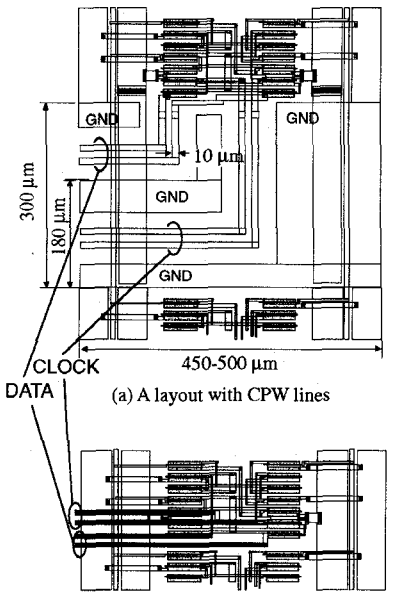
Figure 4: Isolation characteristics of a 500-μm IMSL.

The isolation level of signal-lines with 10-μm space is lees than -30 dB below 40 GHz. The crosstalk between signals is thus almost negligible in 40-Gbit/s ICs with 10-μm spaced signal lines.

The third feature of the IMSL-IC structure is that the impedance-controlled lines can easily be introduced without increasing layout size. Figure 5 compares the layout of a circuit using the IMSL–IC structure with that of one using CPW lines for impedance-matching. The layout with CPW lines needs a large signal line area, comparable to the circuit cell, because all internal signals are differential in high-speed digital ICs. In this case, the chip size exceeds 2.5×2.5 mm, which is the limit size for preventing cavity resonance frequencies below 40 GHz. CPW lines therefore cannot be used in high-speed digital ICs. The IMSL–IC layout, however, is very compact because there is no ground plane between the signal lines and because of the three-dimensional IMSL layout over circuit elements.

High-speed IC Application Examples

Figure 6 shows typical examples of IMSL applications in high-speed digital ICs. In these examples, operation at 40 Gbit/s is assumed. In the DEMUX IC, 20-GHz clock and 40-Gbit/s data signals run in parallel for 500-700 μm. In the MUX IC, a 40-GHz clock signal runs over a path 1,500 μm long.



(a) A layout with CPW lines

(b) A layout with IMSLs

Figure 5: Examples of impedance-controlled line layouts.

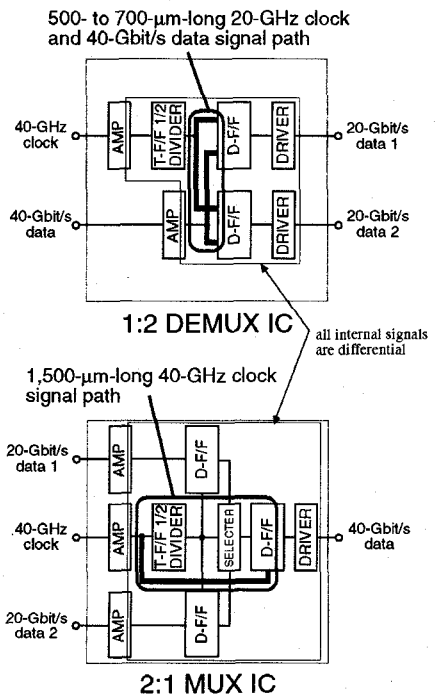


Figure 6: Critical layout patterns in digital ICs.

Figure 7 shows the waveforms simulated for conventional 3-μm line/space lines and for a 10-μm line/space IMSL corresponding to the DEMUX layout in Figure 6. This figure clearly shows the remarkable crosstalk suppression achieved with the IMSL.

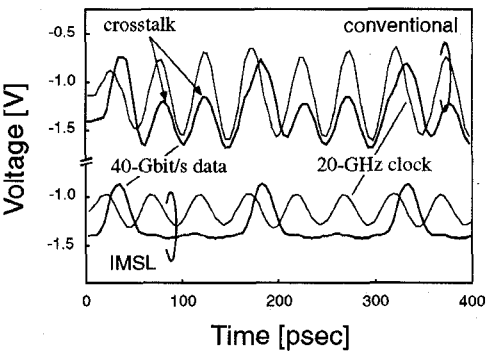


Figure 7: Simulated waveforms of 20-GHz clock and 40-Gbit/s data signals.

Figure 8 compares waveforms simulated of 40-GHz step responses in a conventional line and in an impedance-matched IMSL corresponding to the MUX layout in Figure 6. The waveforms of the conventional line shows a large overshoot and undershoot due to impedance matching miss. These distortions change clock phase, and the timing between clock and data signals is lost. In this case, 40-Gbit/s operation cannot be expected.

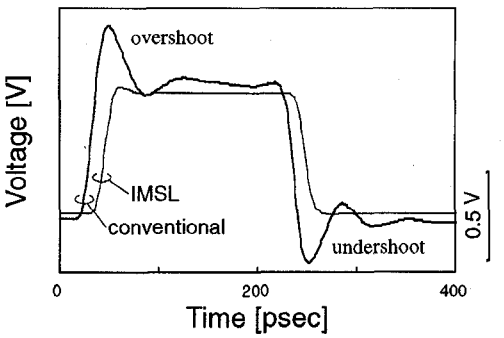


Figure 8: Simulated 40-GHz step responses of clock line.

These results show that the waveform distortion due to crosstalk and impedance matching miss can be remarkably suppressed with the IMSL–IC structure while keeping chip size small.

There is another advantage in using the IMSL–IC structure in digital ICs. This structure enables the use of passive circuit elements, such as a hybrid for single-end to differential signal transformation and a power divider for signal distribution in digital ICs. Such circuits have never been used in digital ICs because their layout size was too large. Figures 9 and 10 show the layout and measured s-parameters of a branch-line hybrid circuit with meandering TPSLs. Its size is reduced to that of common circuit units in digital ICs because of the TPSL's extremely high isolation characteristics. Digital IC performance can be improved by replacing the clock amplifiers with these circuits because the clock is the highest signal and the clock amplifier is one of the bottlenecks in high-speed digital ICs. The use of these passive circuits is expected to increase the flexibility of digital-circuit design.

Conclusion

The novel IMSL-IC structure proposed here has the following features:

- Entire top ground plane of IMSL-IC makes the parasitic-impedance of a module very low and completely eliminates the reduction of signal-line impedance by flip-chip bonding.
- High-isolation IMSL and 3-D layout makes chip size very small and avoids cavity resonance problems.
- The IMSL-IC structure enables impedance-controlled lines and passive circuit elements to be used in digital ICs without increasing chip size. It also improves and stabilizes IC performance and allows new design flexibility.

Acknowledgments

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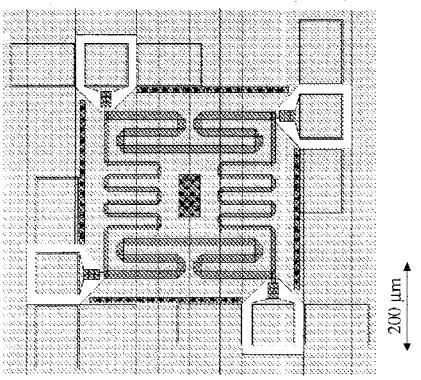

Figure 9: Layout pattern of TPSL branch-line hybrid circuit.

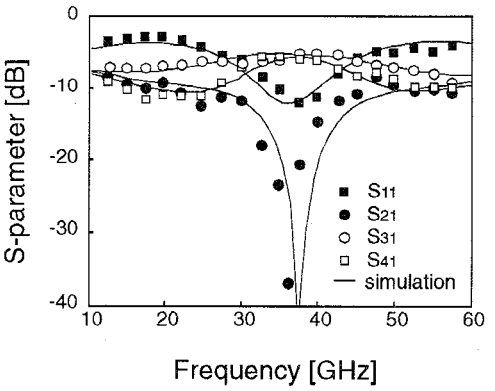

Figure 10: Measured and simulated s-parameters of branch-line hybrid circuit.

References

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[2] M. Hirano, K. Nishikawa, I. Toyoda, S. Aoyama, S. Sugitani, and K. Yamasaki, "Three-Dimensional Passive Circuit Technology For Ultra-Compact MMICs", MTT-S 1995.